



Applicant:

Wrschka, et al.

Docket No.:

2001 P 14591 US

19W

Serial No.:

10/084,194

Art Unit:

2823

Filed:

February 28, 2002

Examiner:

Estrada, Michelle

For:

Integration Scheme for Metal Gap Fill, with Fixed Abrasive CMP

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit:

October 20, 2004

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Certificate of Mailing via First Class Mail (1 page) Election and Preliminary Amendment (5 pages) Information Disclosure Statement (1 page) PTO/SB/08A & B with 13 References Cited (2 pages) Copy of 13 Cited References Return Postcard

Respectfully submitted,

Kristin Hayes

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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INFORMATION DISCLOSURE STATEMENT

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

October 20, 2004

Date

Attorney for Applicant

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2823

PTO/SB/08a (08-03)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE Ander the Paperwood Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number. FIRANFUL Complete if Known te for form 1449A/PTO 10/084,194 Application Number **INFORMATION DISCLOSURE** Filing Date February 28, 2002 STATEMENT BY APPLICANT First Named Inventor Wrschka, et al.

Art Unit

(Use as many sheets as necessary)

Examiner Name Estrada, Michelle Sheet 2 Attorney Docket Number 2001 P 14591 US

U.S. PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	Document Number Number - Kind Code ^{2 (if known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
	1	US-5,692,950	12-02-1997	Rutherford et al.			
	2	US-5,850,105	12-15-1998	Dawson et al.			
	3	US-6,034,418	03-07-2000	Matsuura			
	4	US-6,037,278	03-14-2000	Koyanagi et al.			
	5	US-6,232,171 B1	05-15-2001	Mei			
·····	6	US-6,232,231 B1	05-15-2001	Sethuraman et al.			
	7	US-6,310,375 B1	10-30-2001	Schrems .			
	8	US-6,350,692 B1	02-26-2002	Economikos et al.			
	. 9	US-2002/0074311 A1	06-20-2002	Funkenbusch			
	10	US-2003/0029212 A1	02-13-2003	lm			
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	T6	
		Country Code ³ - Number ⁴ - Kind Code ⁵ (<i>if known</i>)	IVIIVI-UU-TTTT		or Relevant Figures Appear	<u> </u>	
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Substitute for form 1449B/PTO				Complete if Known		
				Application Number	10/084,194	
INF	ORMATION	DISCLO	OSURE	Filing Date	February 28, 2002	
STATEMENT BY APPLICANT				First Named Inventor	Wrschka, et al.	
				Art Unit	2823	
(Use as many sheets as necessary)			ary)	Examiner Name	Estrada. Michelle	
Sheet	2	of	2	Attorney Docket Number	2001 P 14591 US	

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
	11	WOLF, S., Silicon Processing for the VLSI Era, Vol. 2, Lattice Press, Sunset Beach, California (1990) pp. 189- 193.			
	12	PENKA, S., et al., "Integration Aspects of Flowfill and Spin-on-Glass Process for Sub-0.35µm Interconnects," Interconnect Technology Conference, Proceedings of the IEEE 1998 International (June 1-3, 1998) pp. 271-273.			
	13	MENDONCA, J., et al., "Interconnect Material and CMP Process Change Effects on Local Interconnect Planarity," Interconnect Technology Conference, Proceedings of the IEEE 1998 International (1998) pp. 196-198.			

Examiner	Date	
Signature	Considered	
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